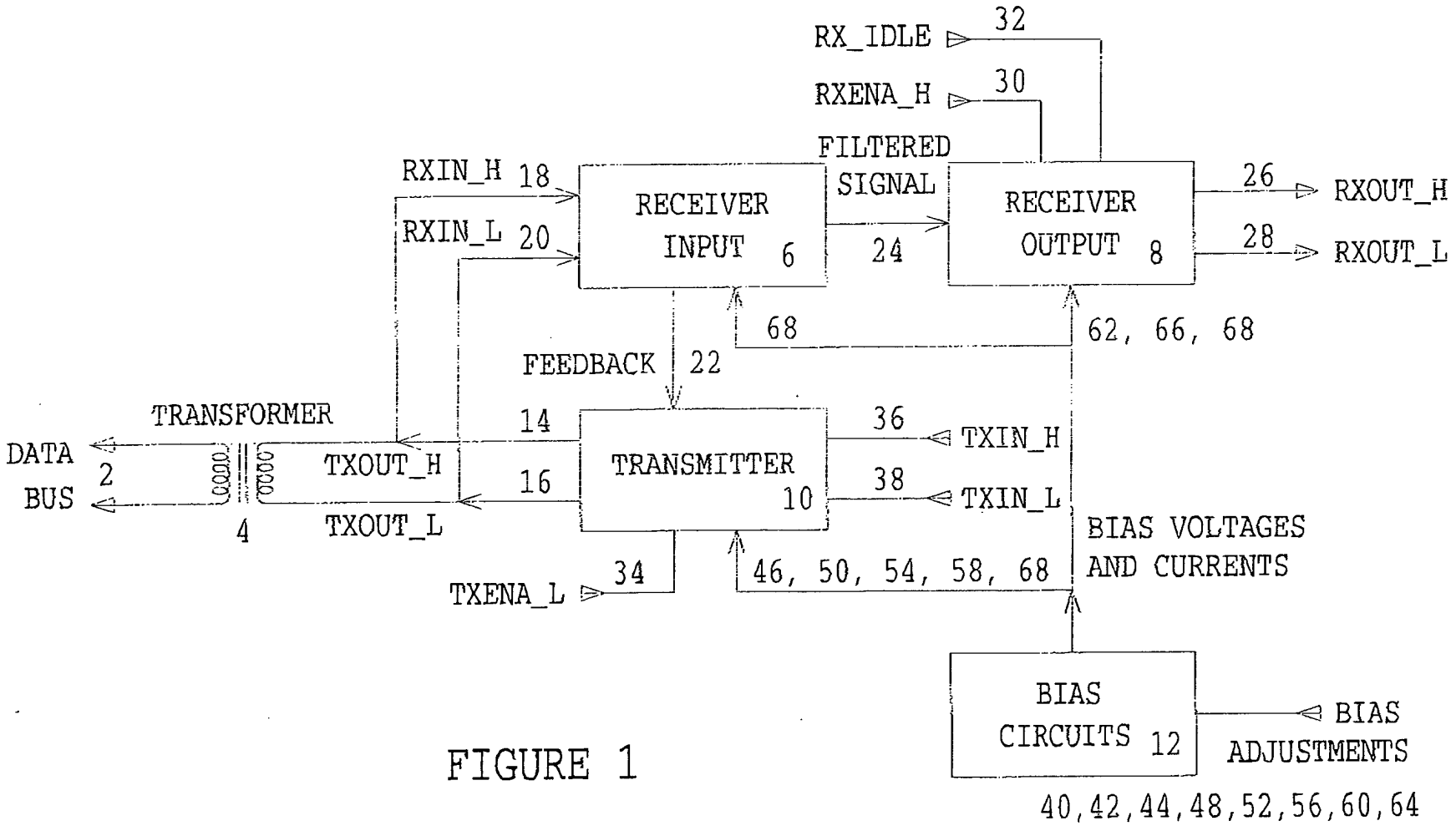

RX_IDLE
32
RXENA_H
30
FILTERED
SIGNAL
RXIN_H
18
RXIN_L
20
RECEIVER
INPUT
6
24
RECEIVER
OUTPUT
8
26
RXOUT_H
28
RXOUT_L
68
62, 66, 68
FEEDBACK
22
TRANSFORMER
DATA
BUS
2
4
14
16
TXOUT_H
TXOUT_L
TRANSMITTER
10
36
TXIN_H
38
TXIN_L
BIAS VOLTAGES
AND CURRENTS
TXENA_L
34
46, 50, 54, 58, 68
BIAS
CIRCUITS
12
BIAS
ADJUSTMENTS
40,42,44,48,52,56,60,64

FIGURE 1

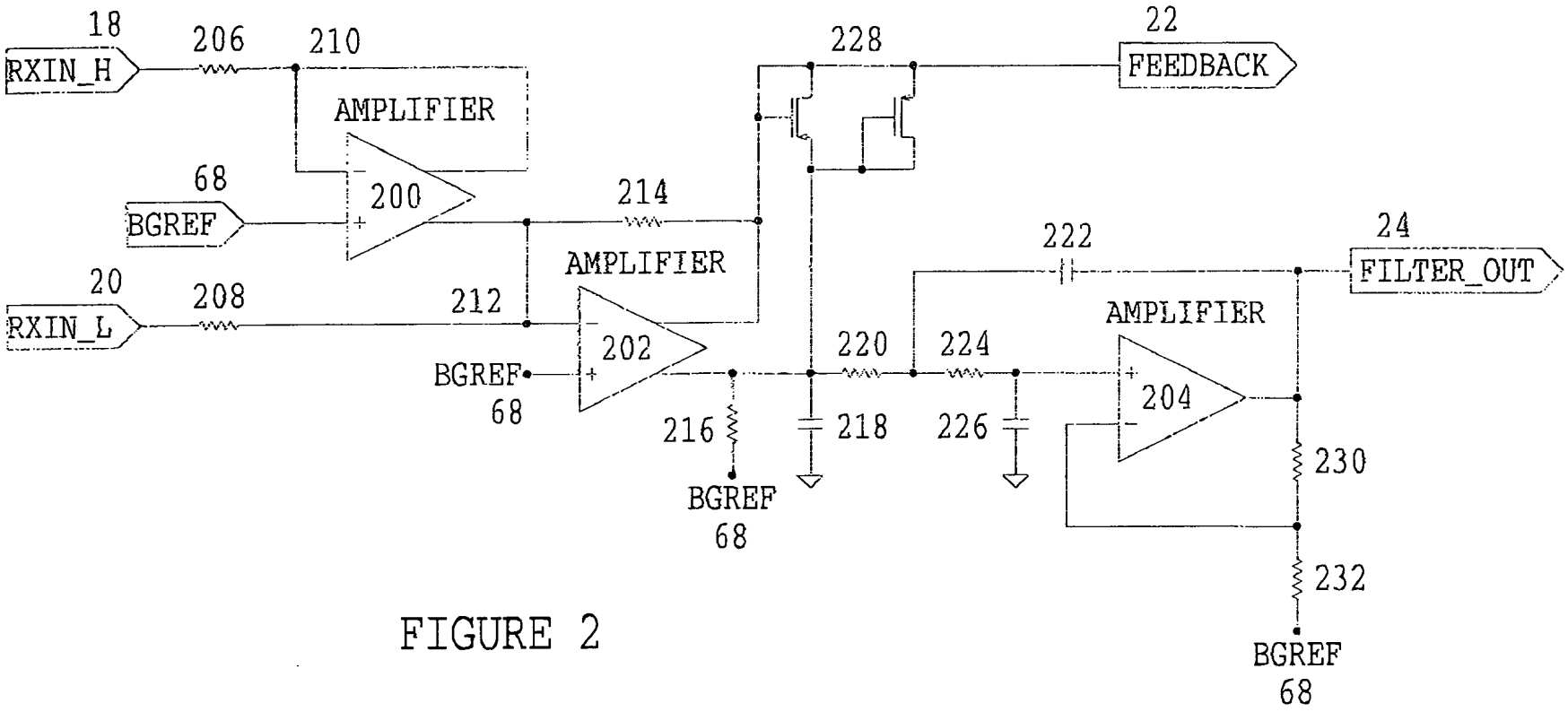


FIGURE 2

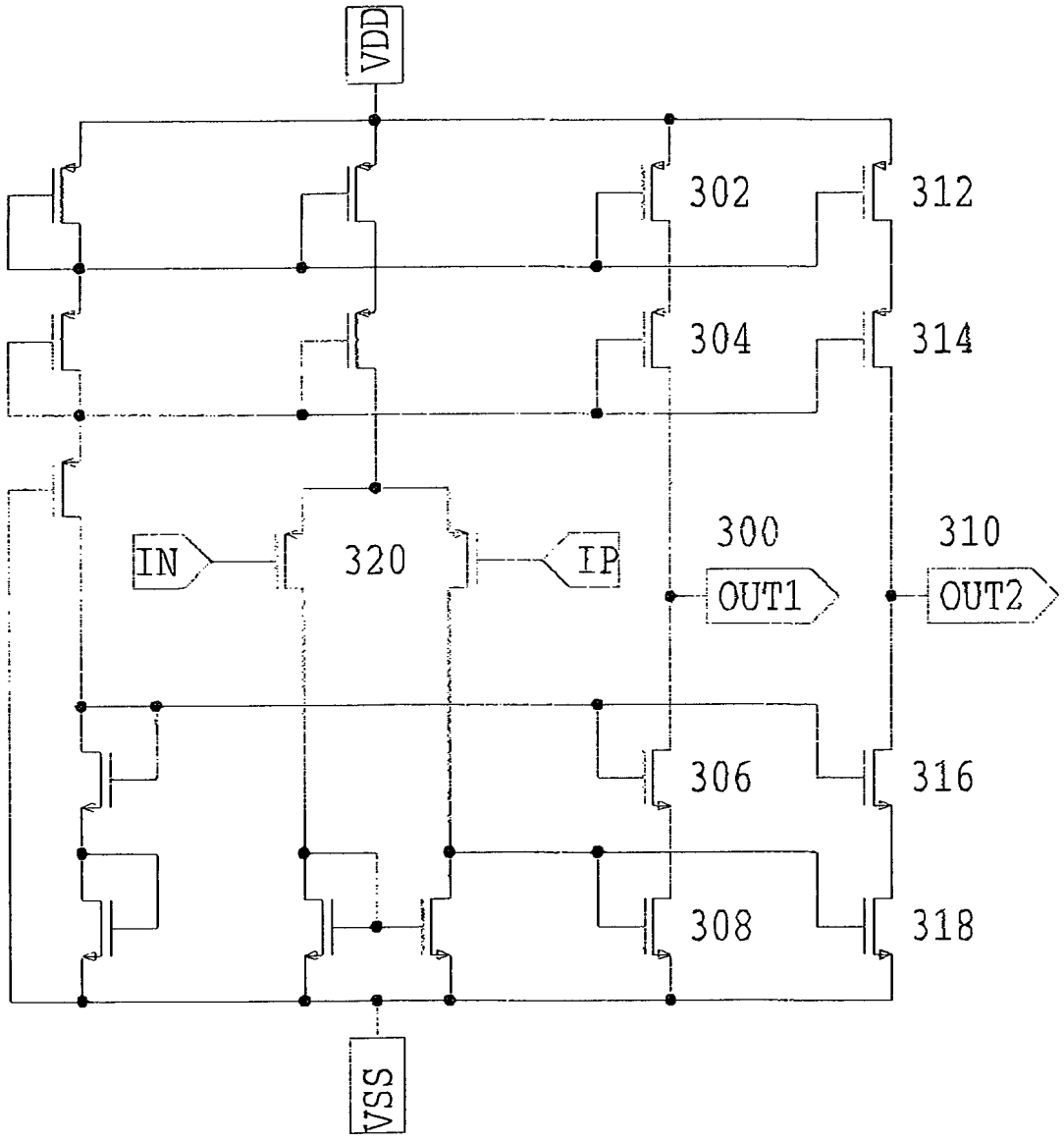

VDD
302
312
304
314
IN
320
IP
300
OUT1
310
OUT2
306
316
308
318
VSS

FIGURE 3

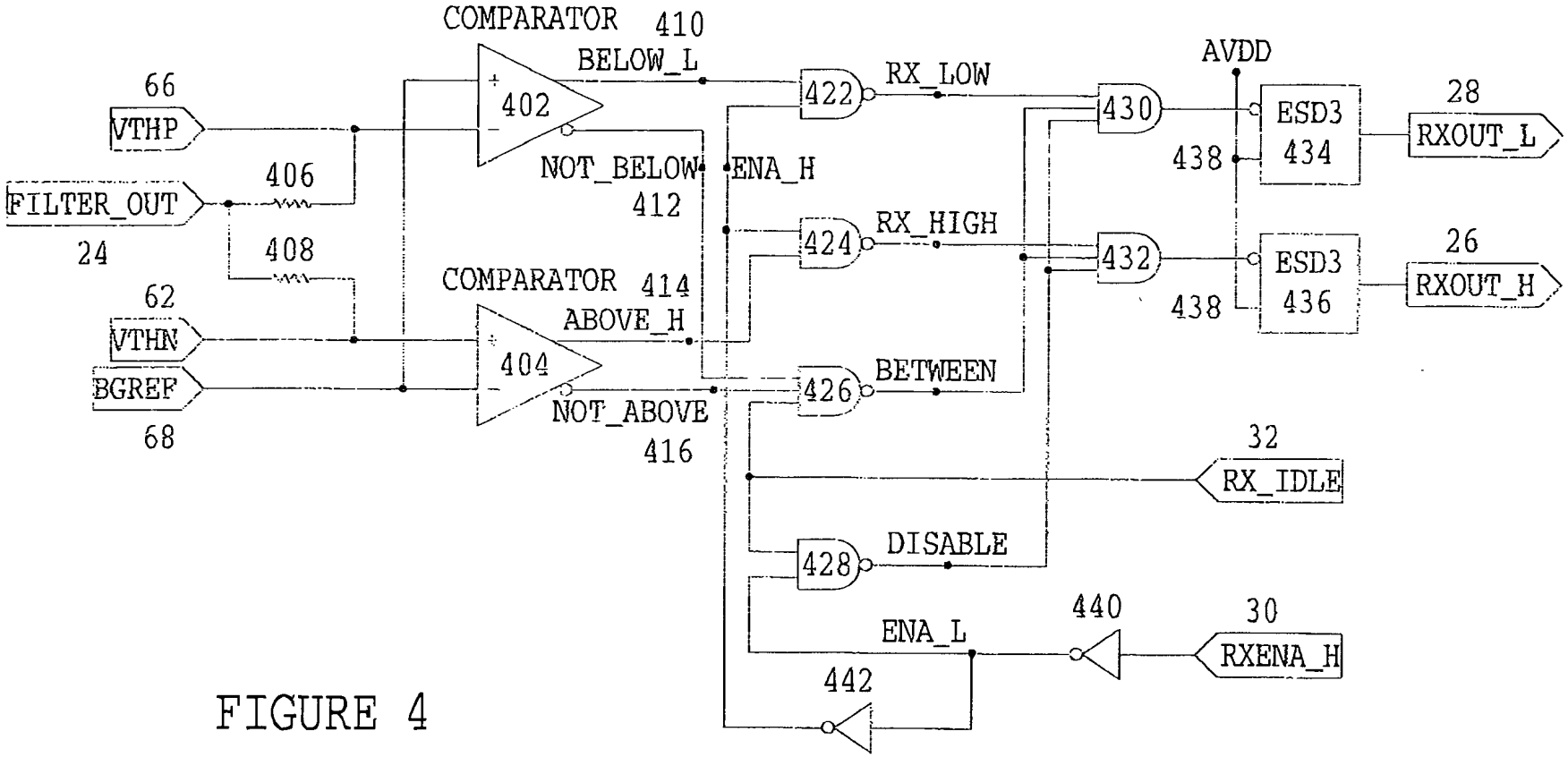
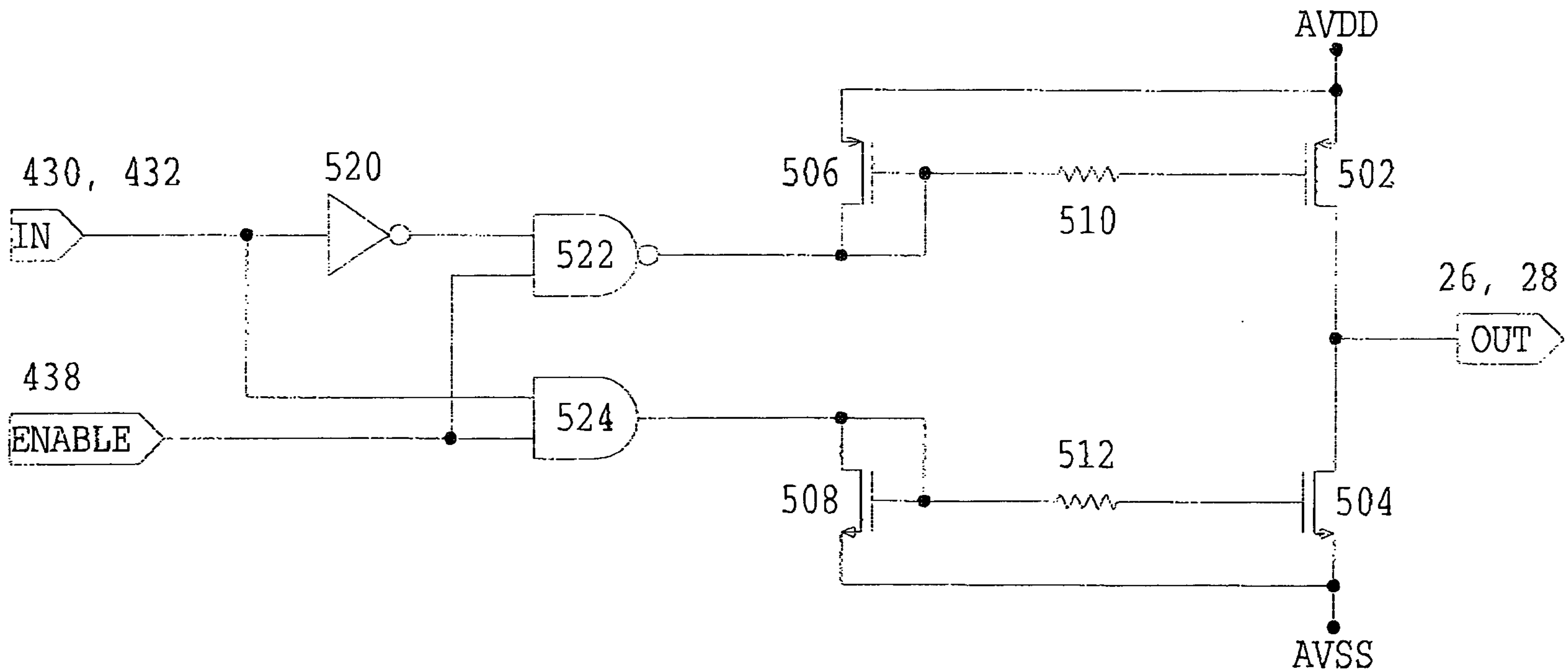


FIGURE 4



AVDD
430, 432
520
506
502
IN
522
510
26, 28
OUT
438
524
512
ENABLE
508
504
AVSS

FIGURE 5

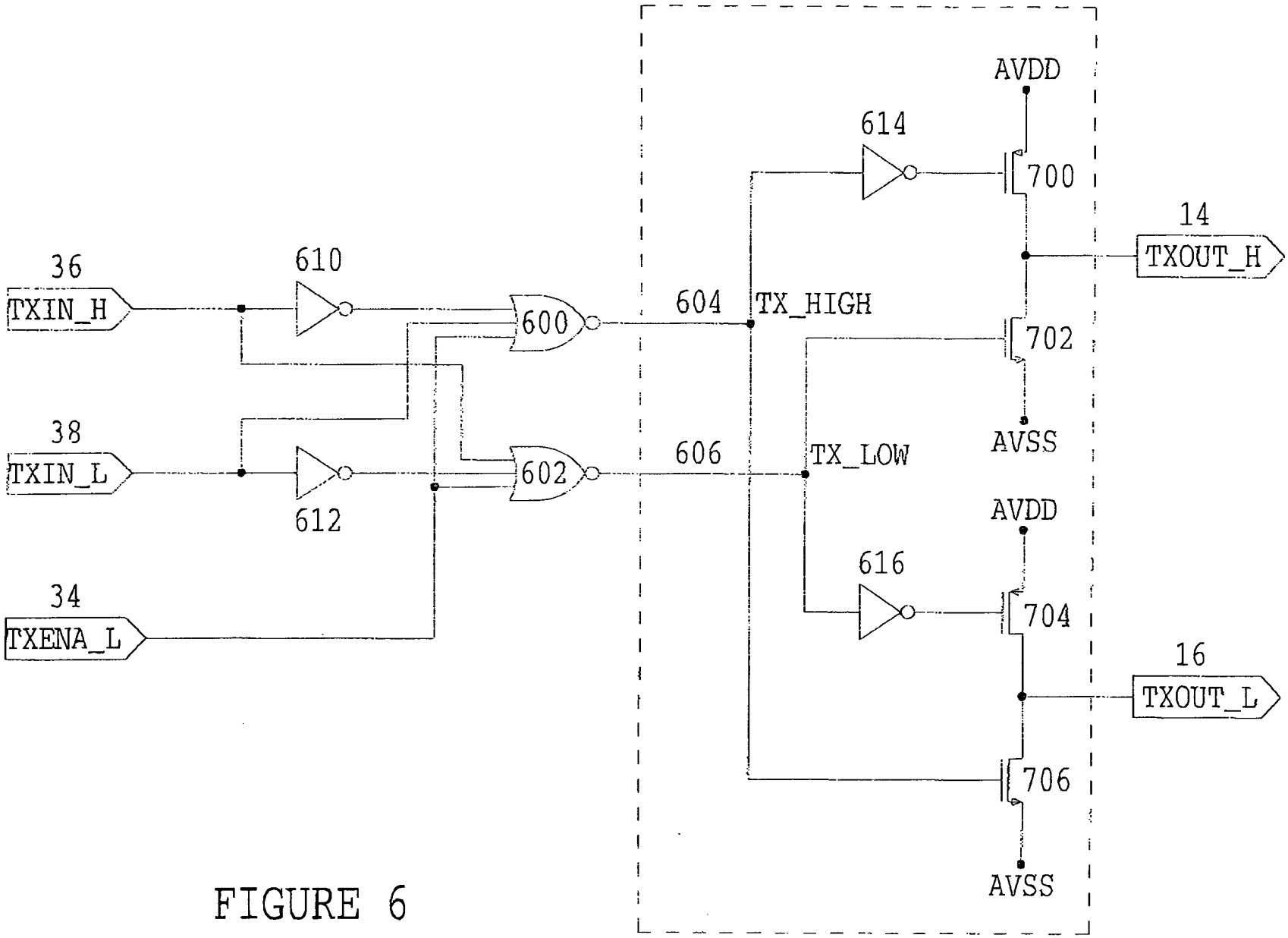


FIGURE 6

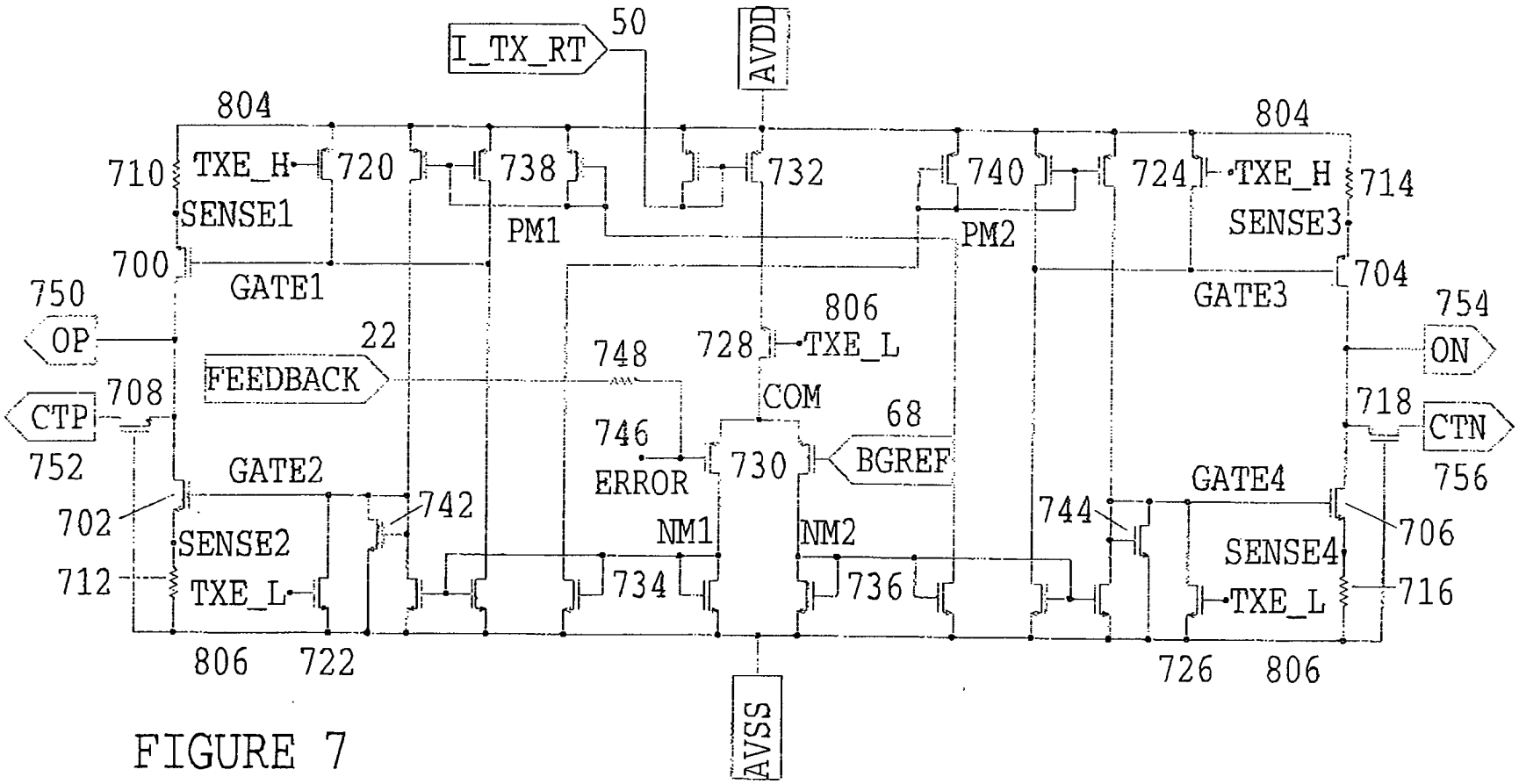

I_TX_RT
50
AVDD
804
804
710
TXE_H
720
738
732
740
724
TXE_H
714
SENSE1
PM1
PM2
SENSE3
700
GATE1
704
GATE3
750
806
754
OP
22
748
728
TXE_L
ON
FEEDBACK
708
COM
718
CTP
746
68
CTN
752
GATE2
730
BGREF
GATE4
756
ERROR
744
702
742
NM1
NM2
706
SENSE2
SENSE4
712
TXE_L
734
736
716
TXE_L
806
722
726
806
AVSS

FIGURE 7

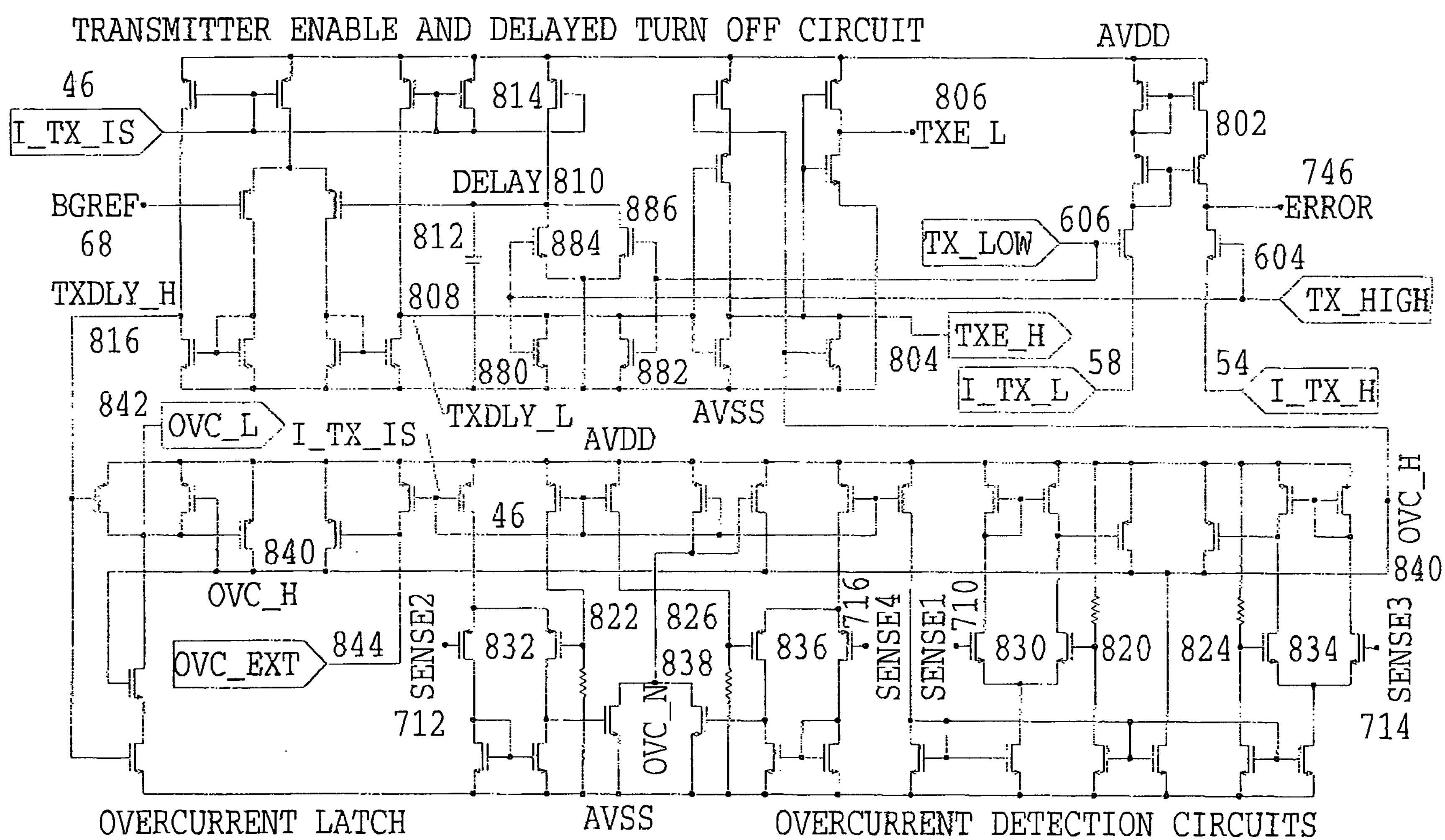

TRANSMITTER ENABLE AND DELAYED TURN OFF CIRCUIT
AVDD
46
I_TX_IS
814
806
TXE_L
802
BGREF
68
DELAY
810
886
884
812
746
ERROR
606
TX_LOW
604
TXDLY_H
816
808
880
882
TX_HIGH
TXE_H
804
58
I_TX_L
54
I_TX_H
842
OVC_L
I_TX_IS
TXDLY_L
AVDD
AVSS
OVC_H
46
840
OVC_H
840
822
826
838
716
SENSE4
SENSE1
710
830
820
824
834
SENSE3
714
844
OVC_EXT
SENSE2
832
712
836
OVC_N
OVERCURRENT LATCH
AVSS
OVERCURRENT DETECTION CIRCUITS

FIGURE 8

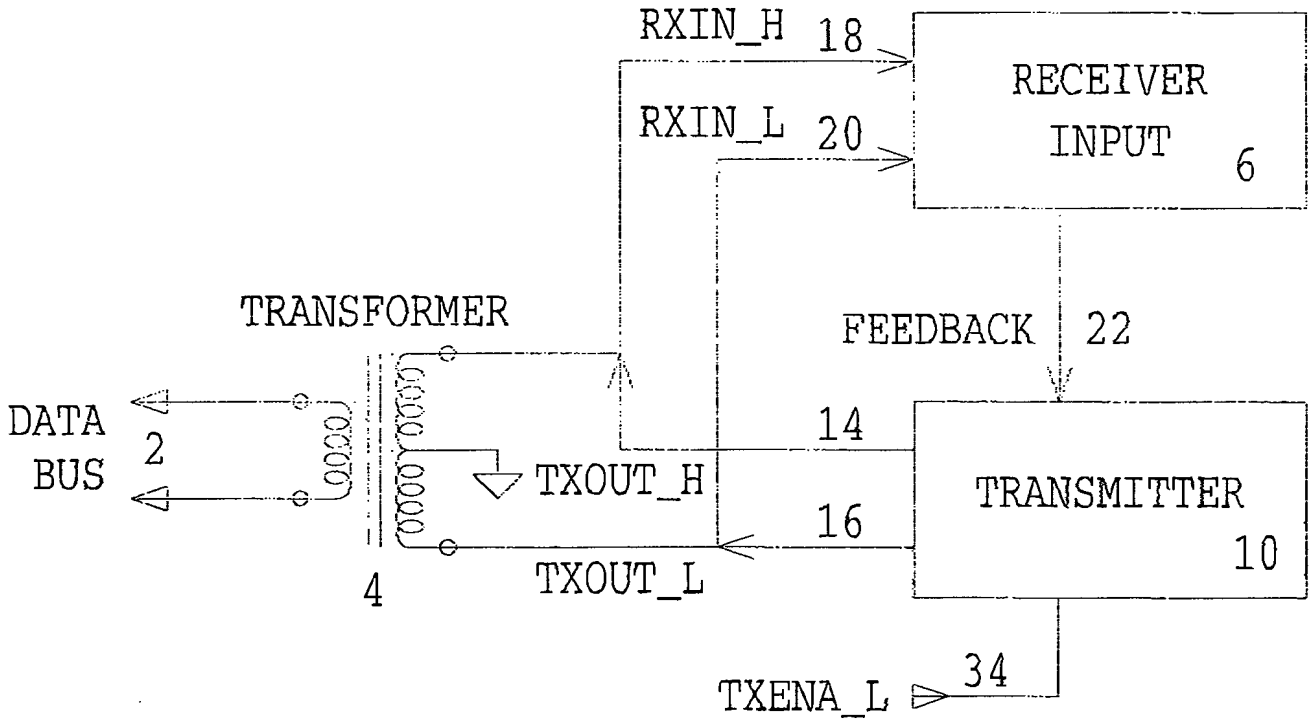


FIGURE 9

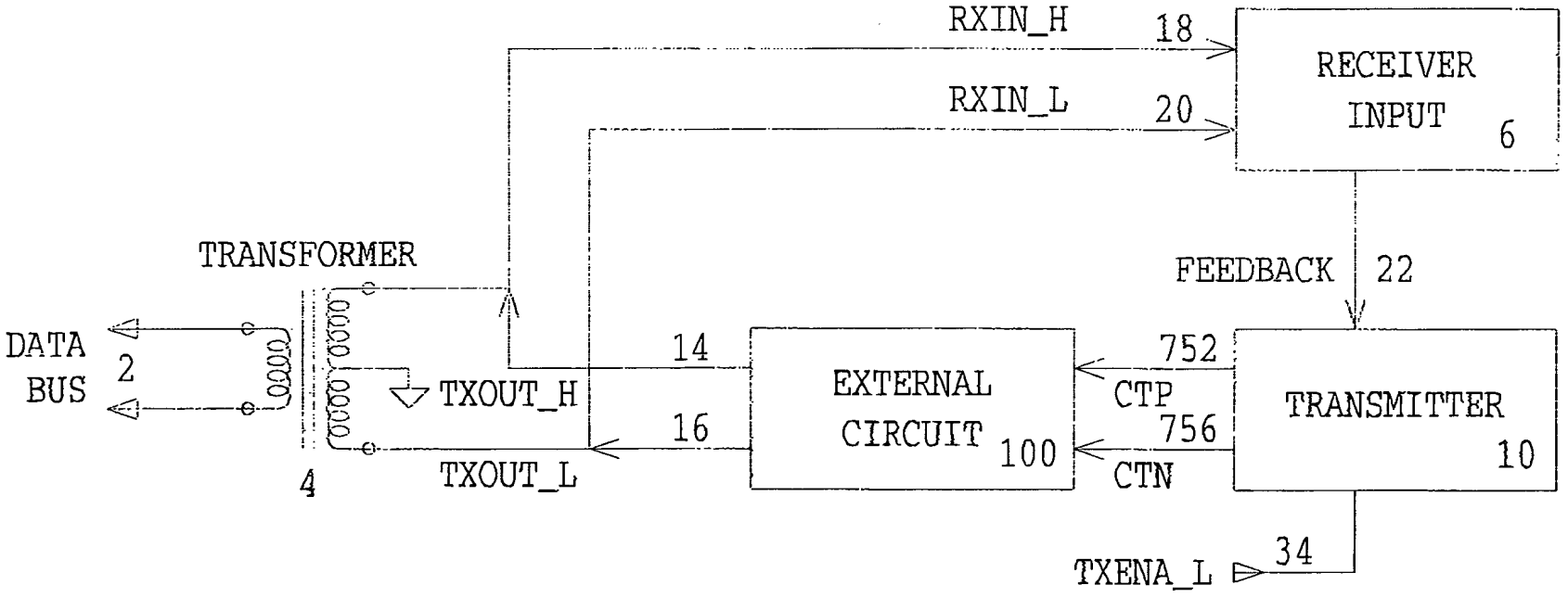


FIGURE 10

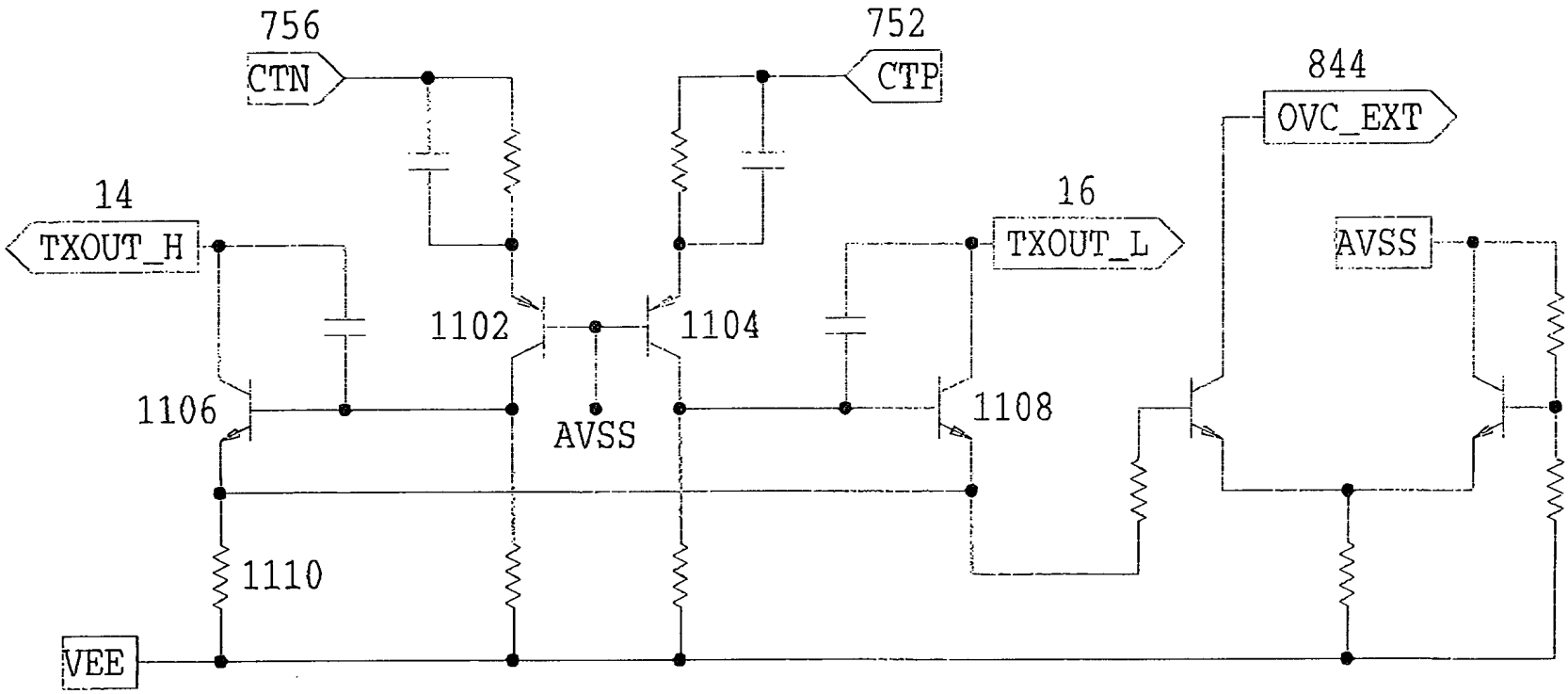


FIGURE 11

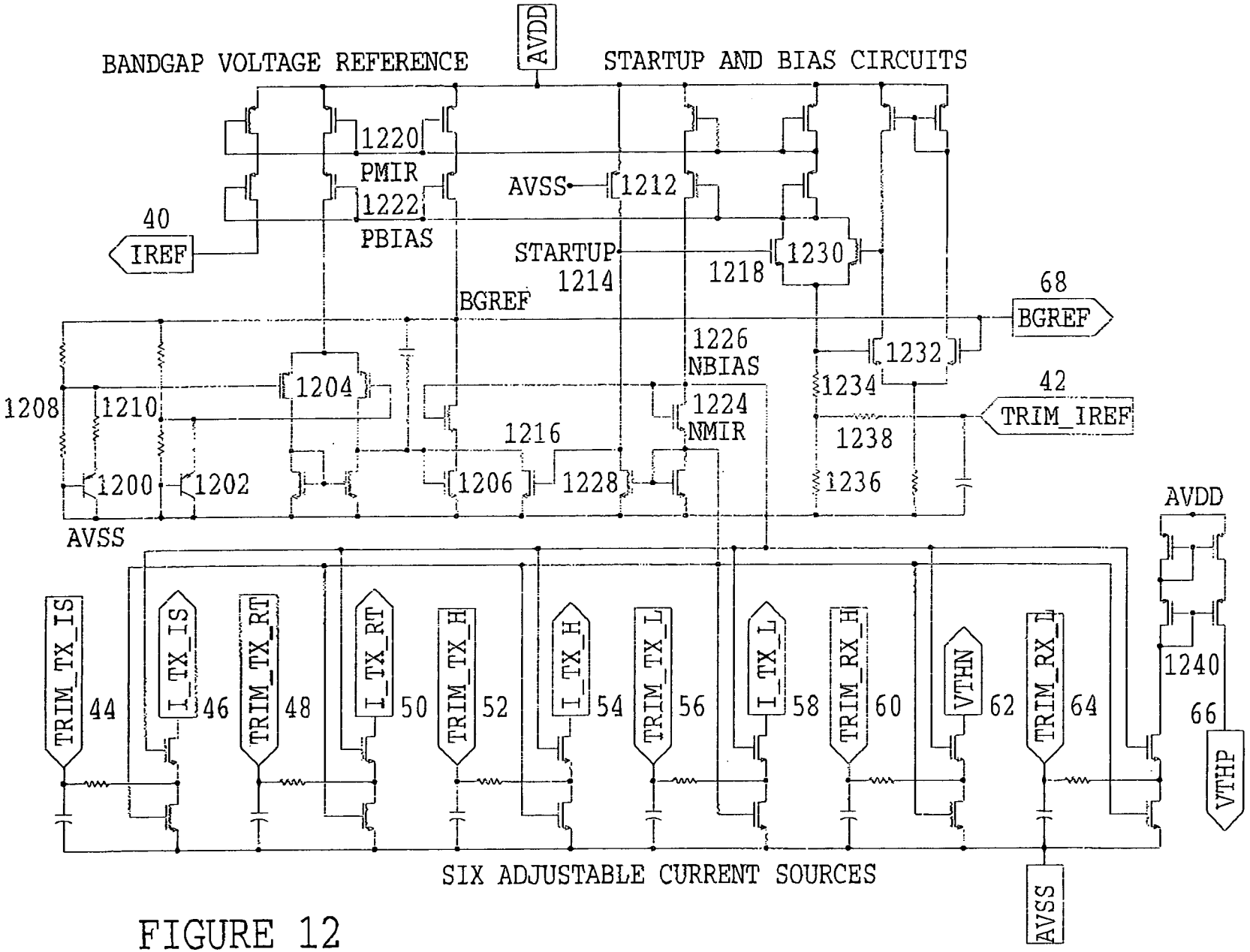


FIGURE 12